IN THE CLAIMS

Please replace the claims with the following set, in which claims 14, 16-18, 20-22, 29, 33, 36, 40, 46, and 52-54 are amended.

Claims 1-13 are withdrawn.

14. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions each having ~~of~~ at least two ~~or more adjacent~~ transistors~~,~~ ~~the active regions having~~ and at least ~~more than one first and second~~ two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate in each active region between ~~more than one first and second~~ the at least two electrodes ~~of those active regions respectively~~, wherein at least two ~~or more~~ transistor gates are of a predetermined width and length ~~at~~ and separated by a substantially identical gap ~~therebetween without intervening dummy gates therebetween~~ with no intervening structures between the at least two transistor gates; and

a plurality of dummy gates having the predetermined width and length and located between ~~ones of the adjacent~~ the at least two transistors, wherein at least two dummy gates are separated from an adjacent transistor gate by the ~~at a~~ substantially identical gap, and wherein the plurality of dummy gates are separated from each other by the substantially identical gap ~~therebetween, without intervening transistor gates therebetween, respectively~~.

15. (Previously amended) The device, as defined in claim 14, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

16. (Currently amended) The device, as defined in claim 14, wherein at least ~~more than one~~ two gate transistors of ~~a plurality~~ each of the at least two transistors ~~respectively have~~ has a common terminals~~, each of which is~~ the common terminal commonly connected on the substrate.

17. (Currently amended) The device, as defined in claim 14, wherein ~~a~~ the plurality of dummy gates ~~are~~ is commonly connected on the substrate.

18. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of~~ comprising at least two ~~or more adjacent~~ transistors, the active regions having at least ~~more than one~~ two ~~first and second~~ electrodes disposed on the substrate;

a plurality of transistor gates disposed between ~~more than one first and second~~ the at least two electrodes ~~of those active regions~~, the transistor gates being positioned such that at least ~~more than one~~ two transistor gates ~~is~~ are of a predetermined width and length ~~at~~ with a substantially identical gap ~~therebetween without intervening dummy gates therebetween~~ separating the at least two transistor gates with no intervening structures between the at least two transistor gates; and

a plurality of dummy gates having the predetermined width and length and located between and to either side ~~outside ones~~ of the at least two ~~adjacent~~ transistors, wherein at least four dummy gates are separated from an adjacent transistor gate by the ~~at a~~ substantially identical gap, and wherein each of the plurality of dummy gates is separated from another dummy gate by the substantially identical gap ~~therebetween, without intervening transistor gates therebetween, respectively~~.

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19. (Previously amended) The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

20. (Currently amended) The device, as defined in claim 18, wherein at least ~~more than one~~ two gate transistors of ~~a plurality~~ each of the at least two transistors ~~respectively have~~ has a common terminals, ~~each of which is~~ the common terminal commonly connected on the substrate.

21. (Currently amended) The device, as defined in claim 18, wherein ~~a~~ the plurality of dummy gates ~~are~~ is commonly connected on the substrate.

22. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of~~ comprising at least two ~~or more adjacent~~ transistors having at least more than one first and second two electrodes disposed on the substrate;

a plurality of transistor gates disposed between ~~more than one first and second~~ the at least two electrodes ~~of those active regions~~, the transistor gates being positioned such that at least ~~more than one~~ two transistor gates ~~has~~ have a predetermined width and length ~~at~~ with a substantially identical gap ~~therebetween without intervening dummy gates therebetween~~ separating the at least two transistor gates with no intervening structures between the at least two transistor gates; and

a plurality of dummy gates having the predetermined width and length and located not between but to both sides ~~outside ones~~ of the ~~adjacent~~ at least two transistors, wherein at least two dummy gates are separated from an adjacent transistor gate by the ~~at a~~ substantially identical gap, and wherein each of the plurality of dummy gates is separated from another dummy gate by the substantially identical gap ~~therebetween, without intervening transistor gates therebetween, respectively~~.

23. (Original) The device, as defined in claim 22, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

24. (Original) The device, as defined in claim 22, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

25. (Original) The device, as defined in claim 22, wherein a plurality of dummy gates are commonly connected on the substrate.

29. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions on the substrate each having a source region and a drain region ~~on the substrate~~;

a portion on the substrate other than the active region ~~on the substrate~~;

a plurality of transistor gates formed on the active regions, the gates being disposed between the source region and the drain region and having a first gap between adjacent transistor gates, ~~without~~ with no intervening structures between the transistor gates ~~dummy gates therebetween~~;

a plurality of dummy gates formed on the portion other than the active region, the dummy gates being characterized by a second gap between adjacent dummy gates ~~, without~~

~~intervening transistor gates therebetween, respectively~~ and a third gap between at least two dummy gates and a corresponding adjacent transistor gate;

wherein the first, second, and third gap ~~is~~ are substantially identical ~~to the first gap~~.

30. (Previously added) The device, according to claim 29, in which a first metal is connected to the source region and the drain region by a plurality of contacts.

31. (Previously added) The device, according to claim 30, in which a second metal is connected to a first part of the first metal to supply a voltage.

32. (Previously added) The device, according to claim 31, in which the plurality of dummy gates are commonly connected by a second part of the first metal to supply a ground voltage.

33. (Currently amended) A semiconductor device comprising

a substrate;

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a first region having a plurality of first active regions each having a source region and a drain region respectively and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region respectively and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first transistor gates being characterized by a first gap between neighboring first transistor gates~~,~~ and without intervening ~~transistor gates therebetween~~ structure between neighboring first transistor gates;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second transistor gates also being characterized by the first gap between neighboring second transistor gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring first dummy gates~~,~~ and without intervening first transistor gates ~~therebetween~~ between neighboring first dummy gates;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring second dummy gates without intervening second transistor gates ~~therebetween~~ between neighboring second dummy gates;

wherein a first transistor gate at an edge of the first active regions is separated from a first dummy gate at an edge of the first portion by a third gap, wherein a second transistor gate at an edge of the second active region is separated from a second dummy gate at an edge of the second portion by a fourth gap, and wherein the first, second, third, and fourth gaps are substantially identical;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

34. (Previously added) The semiconductor device according to claim 33, in which the first gap is substantially identical to the second gap.

35. (Previously added) The semiconductor device according to claim 33, in which the second metal is connected to a second part of the first metal to supply a ground voltage.

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36. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of two or more adjacent~~ having at least two transistors~~, without intervening transistors therebetween, the active regions having~~ and at least ~~more than one first and second~~ two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between ~~more than one first and second~~ the at least two electrodes of ~~those~~ the active regions, the plurality of transistor gates being characterized by a predetermined first dimension and a variable second dimension ~~on the substrate~~; and

a plurality of dummy gates disposed on the substrate between ~~more than one first and second~~ the at least two electrodes of ~~those~~ the active regions, the plurality of dummy gates being characterized ~~by dummy gates that~~ as substantially filling ~~the~~ a region on the substrate devoid of transistor gates ~~in the second dimension~~;

wherein the plurality of transistor gates have substantially identical first and second dimensions.

37. (Previously added) The semiconductor device according to claim 36, in which the first dimension characterizes a transistor gate length.

38. (Previously added) The semiconductor device according to claim 37, in which the second dimension characterizes a transistor gate width.

39. (Previously amended) The semiconductor device according to claim 36, in which adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

40. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of two or more adjacent~~ having at least two transistors~~,~~ ~~the active regions having at least more than one first and second~~ and two electrodes disposed on the substrate;

a plurality of transistor gates of a first width disposed on the substrate between ~~more than one first and second~~ the at least two electrodes of ~~those~~ the active regions ~~respectively, wherein two or more transistor gates are of an elongated length relative to width~~; ~~and~~

a plurality of dummy gates of a second width disposed on the substrate between the at least two electrodes of the active regions; and ~~having an elongated length relative to width and located and oriented in aligned opposition to the transistor gates~~.

a plurality of dummy gates of a third width disposed on the substrate between the at least two electrodes of the active regions, wherein each of the transistor gates is aligned along the same longitudinal axis as a corresponding one of the dummy gates of a third width, and wherein the second width is greater than the sum of the first and third widths.

41. (Previously added) The semiconductor device according to claim 40, in which the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

42. (Previously added) The device, as defined in claim 40, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

43. (Previously added) The device, as defined in claim 40, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

44. (Previously added) The device, as defined in claim 40, wherein a plurality of dummy gates are commonly connected on the substrate.

45. (Previously added) The device, as defined in claim 40, wherein the width of the dummy gates is substantially the same as that of the transistor gates.

46. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of~~ having at least two ~~or more adjacent~~ transistors~~, the active regions having~~ and at least ~~more than one first and second~~ two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between ~~more than one first and second~~ the at least two electrodes of ~~those~~ the active regions ~~respectively~~, wherein ~~two or more~~ at least two transistor gates ~~are of~~ have an elongated length relative to width; and

a plurality of dummy gates disposed on the substrate, having a first portion in contact with a bias line, and having at least one ~~or more~~second portions extending in a vertical direction and ~~disposed on the substrate~~ arranged such that the at least one ~~or more~~ second portions ~~are~~ is interspaced between adjacent transistor gates.

47. (Previously added) The semiconductor device according to claim 46, in which the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

48. (Previously added) The device, as defined in claim 46, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

49. (Previously added) The device, as defined in claim 46, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

50. (Previously added) The device, as defined in claim 46, wherein a plurality of dummy gates are commonly connected on the substrate.

51. (Previously added) The device, as defined in claim 46, wherein the width of the dummy gates is substantially the same as that of the transistor gates.

52. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of two or more adjacent~~ having at least two transistors~~, the active regions having~~ and at least ~~more than one first and second~~ two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between ~~more than one first and second~~ the at least two electrodes of ~~those~~ the active regions ~~respectively~~, ~~wherein two or more transistor gates are of an elongated length relative to width~~ at least two transistor gates have a first portion extending in a first direction and a plurality of second portions extending in a second direction perpendicular to the first direction; and

D1 a plurality of dummy gates ~~having an elongated length relative to width and aligned in vertical opposition to the transistor gates~~ disposed on the substrate between the at least two electrodes of the active regions, ~~the length of the dummy gates being substantially the same as that of the transistor gates~~ each dummy gate having a first portion extending in the first direction and a plurality of second portions extending in the second direction perpendicular to the first direction;

wherein a gap between adjacent second portions of the at least two transistor gates and a gap between adjacent second portions of the dummy gates are substantially identical to a gap between a second portion of a transistor gate and an adjacent second portion of a dummy gate ~~the plurality of transistor gates and the plurality of dummy gates are of substantially identical gap between gates~~;

wherein a physical dimension of the second portions of the at least two transistor gates in the first direction is substantially identical to a physical dimension of the second portions of the plurality of dummy gates in the first direction;

and wherein the plurality of transistors gates and the plurality of dummy gates are commonly connected on the substrate, respectively.

53. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of~~ having at least two ~~or more adjacent~~ transistors~~, the active regions having~~ and at least ~~more than one first and second~~ two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between ~~more than one first and second~~ the at least two electrodes of ~~those~~ the active regions ~~respectively~~, at least two transistor gates having a first portion extending in a first direction and a plurality of second portions extending in a second direction perpendicular to the first direction ~~wherein two or more gates are of an elongated length relative to width~~; and

a plurality of dummy gates, each having a first portion extending in the first direction and in contact with a bias line, each having ~~and one or more~~ at least one second portions extending in ~~a vertical~~ the second direction and disposed on the substrate such that the at least one ~~or more~~ second portions ~~are~~ is interspaced between ~~adjacent transistor gates~~ the at least two transistors~~, the length of the dummy gates being substantially the same as that of the transistor gates~~,.

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wherein a gap between adjacent second portions of the at least two transistor gates and a gap between adjacent second portions of the dummy gates are substantially identical to a gap between a second portion of a transistor gate and an adjacent second portion of a dummy gate ~~the plurality of transistor gates and the plurality of dummy gates are of substantially identical gap between gate~~;

wherein a physical dimension of the second portions of the at least two transistor gates in the first direction is substantially identical to a physical dimension of the second portions of the plurality of dummy gates in the first direction;

and wherein the plurality of transistors and the plurality of dummy gates are commonly connected on the substrate, respectively.

54. (Currently amended) A semiconductor device comprising:

a substrate;

a rectangular region on the substrate;

an active region having a first width and a second width on said rectangular region;

an isolation portion of said active region on said rectangular region;

first transistor gates on said first width of said active region;

second transistor gates on said second width; and

first dummy gates on said isolation portion aligned with said first transistor gates such that a portion of a first dummy gate extending in a first direction and a portion of a corresponding first transistor gate extending in the first direction share a common central axis;

wherein said first width is less than said second width;

and wherein said transistor gates and said first dummy gates are of substantially identical gap between gates.

55. (Previously added) The device of claim 54 wherein said active region is n-type.

56. (Previously added) The device of claim 54 wherein said active region is p-type.

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57. (Previously added) The device of claim 54, further comprising:
second dummy gates on said rectangular region having a substantially identical width as said second transistor gates.

58. (Previously added) The device of claim 57 wherein said active region is n-type.

59. (Previously added) The device of claim 57 wherein said active region is p-type.